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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,324	05/18/2005	Mark J. Childs	1217/220	5728

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EXAMINER	
CHOW, YUK	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,324	CHILDS, MARK J.	
	Examiner	Art Unit	
	YUK CHOW	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochi et al. (US 2003/0107537) in view of Nakamura (US 6,867,757).

As to **claim 1**, Ochi discloses a colour active matrix electroluminescent display device comprising a row and column array of display pixels [1], each pixel comprising

an electroluminescent display element [2] (Fig. 1(1R)) and

a drive transistor [22] for driving a current through the display element (Fig. 7(11R)),

the drive transistor and the display element being connected in series between a power line [26] for supplying or drawing a controllable current to or from the display element and a common potential line [30] (see [0022] and Fig. 7),

wherein each row of display pixels comprises different colour display pixels for producing different colour light outputs (See Fig. 7(RGB)),

However, Ochi does not teach wherein the display pixels of each colour in a row are associated with a respective and separate power line [26', 26", 26"'], wherein the

power supply to each power line is individually switchable [40, 45, 48] so as to control the duty cycle of the associated display pixels.

Nakamura discloses a display device wherein teaches the pixels of each colour are associated with a respective and separate power line (see Fig. 1, each color is associated with a separate PWM), Wherein the PWM to each power line is individually switchable (see Fig. 1(108, 109 and 110)).

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to use separate power line to drive each color of a pixel as in Nakamura into display device of Ochi, because this method of controlling a display device capable of maintaining intensity of brightness regardless of a display color, which is an improvement over Ochi (see Nakamura Col. 1 lines 50-55).

As to **claim 2**, Ochi and Nakamura disclose a display device according to claim 1, wherein the power lines [26', 26", 26"'] associated with the rows of pixels are connected to a power supply [40] (see Nakamura Fig. 1(PWM)) through a switching arrangement [45] at one end of the rows.

As to **claim 3**, Ochi and Nakamura disclose a display device according to claim 2, wherein the power lines associated with a row of pixels are connected to at least one power supply rail through respective switches [36, 37, 38] (See Nakamura Fig. 1(108, 109, 110)) of the switching arrangement [45].

As to **claim 4**, Ochi and Nakamura disclose a display device according to claim 3, wherein the number of power supply rails corresponds to the number of power lines

associated with a row of pixels and the power supply rails are shared by all the rows of pixels (see Nakamura Fig. 1 and Col. 3 lines 23-60).

As to **claim 10**, Ochi and Nakamura disclose a display device according to claims 2, wherein the switching arrangement is fabricated on a substrate of the device carrying the display pixels and power lines (see Ochi Fig. 4 and 5, although Ochi does not explicitly state that switching arrangement is fabricated on a substrate, it is a well known in the art to fabricate switching arrangement on a substrate, also it is inherent to place functionally related components near-by or in a group, so that simplified routing improves switching speed and keep the cost of the fabrication down).

As to **claim 11**, Ochi and Nakamura disclose a display device according to claim 1, wherein each row of display pixels comprises red, green, and blue pixels, the different colour pixels being connected to respective power lines (see Nakamura Fig. 1, each color is associated with a separate PWM).

As to **claim 12**, Ochi and Nakamura disclose a display device according to claim 1, wherein the power supply to the power lines for the display pixels of same colour in different rows are individually switchable (see Fig. 1, each color is associated with a separate PWM, and individually switchable via 108, 109 and 110 switches) so as to separately control the duty cycle of each row of display pixels of the same colour (see Nakamura Fig. 4A).

3. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochi and Nakamura (US 6,867,757) in further view of Nakamura (US 2003/0043132).

As to **claim 5**, Ochi and Nakamura '757 disclose a display device according to claim 3 above.

However, Ochi and Nakamura '757 do not explicitly teach each frame period [T_f] each row of pixels is arranged to be addressed in sequence in a respective row address period [T_r] so as to store a drive signal for controlling the operation of the drive transistor [22] of the pixels.

Nakamura '132 discloses a display device wherein teaches control signals consists of frame period (Fig. 3(T2)) is to be addresses in sequence in a respective row address period (Fig. 3(scanning signal (n, n+1…)), also to store a drive signal in a latch circuit (see Fig. 2(24B)).

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to use sequential distribution of signal as in Nakamura into display device of Ochi, due to the fact that sequential driving technique are common and simple to control (see Nakamura '132 [0009]-[0010]).

As to **claim 6**, Ochi and Nakamura disclose a display device according to claim 5, wherein the switching arrangement [45] is operable to connect each of the power lines associated with a row of pixels to the power supply [40] for a predetermined period following addressing which determines the duty cycle of the display pixels associated with the power line, the power lines of each row of pixels being switched in similar manner in sequence (see Nakamura '132 Fig. 3(ASW1, ASW2, ASW3) and [0044]).

As to **claim 7**, Ochi and Nakamura disclose a display device according to claim 6, wherein the power lines of a row are connected to the power supply [40] for a

predetermined period that immediately follows the row address period [T_f] (see Nakamura '132 Fig. 3(ASW1, ASW2, ASW3) for a predetermined period follows the row address (n-th) scanning line).

As to **claim 8**, Ochi and Nakamura disclose a display device according to claims 5, wherein each pixel includes a storage capacitor [24] (see Nakamura '132 Fig. 1(18)) for storing a gate voltage of the drive transistor [22] (Fig. 1(17)) and an address transistor [16] (Fig. 1(13)) for switching a data voltage to the gate of the drive transistor during the row address period, and wherein the switching arrangement [45] is operable to disconnect the power lines of a row of pixels from the power supply during the row address period (see Nakamura '132 Fig. 2 and [0039]).

As to **claim 9**, Ochi and Nakamura disclose a display device according to claims 5, wherein the pixels each include a current sampling circuit for sampling a drive current during the row address period and a storage capacitor for storing a gate--source voltage for the drive transistor corresponding to the sampled drive circuit and wherein the switching arrangement is operable to connect the power lines associated with a row of pixels to the power supply during the row address period (It's well known that pixel circuit using additional circuit for monitoring or ageing compensation, since this is a current-addressed type pixel display circuit, see Nakamura '132 [0035]-[0038], it's inherent to include a current sampling circuit).

Response to Arguments

4. Applicant's arguments filed 03/09/2009 have been fully considered but they are not persuasive.

Regarding claim 1, applicant argues that *Nakamura I* does not teach "the power supply to each power line is individually switchable so as to control the duty cycle of the associated display pixels". However, examiner respectfully disagrees, referring to specification of Nakamura I, Col. 3 lines 50-55, it clearly describes individual switching of transistors 108, 109 and 110, which are individually adjusted by the duty cycle or output of PWMs. The switching is done by the each transistor which is controlled by individual PWM (Fig. 1(105-106). Each color pixel can be individually switched on or off for different duty cycle (see Fig. 4A-4C).

Applicant further argues that *Nakamura I* does not teach the individually switchable power lines. However, examiner disagrees, Fig. 1 describes three current paths going through RBG pixels, for example, one of them is from VDD through 101, 108, then to the ground , and each power line/path is switchable via transistor.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YUK CHOW whose telephone number is (571)270-1544. The examiner can normally be reached on 8-6 M-TH E.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. C./
Examiner, Art Unit 2629

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629